Angel Velazquez

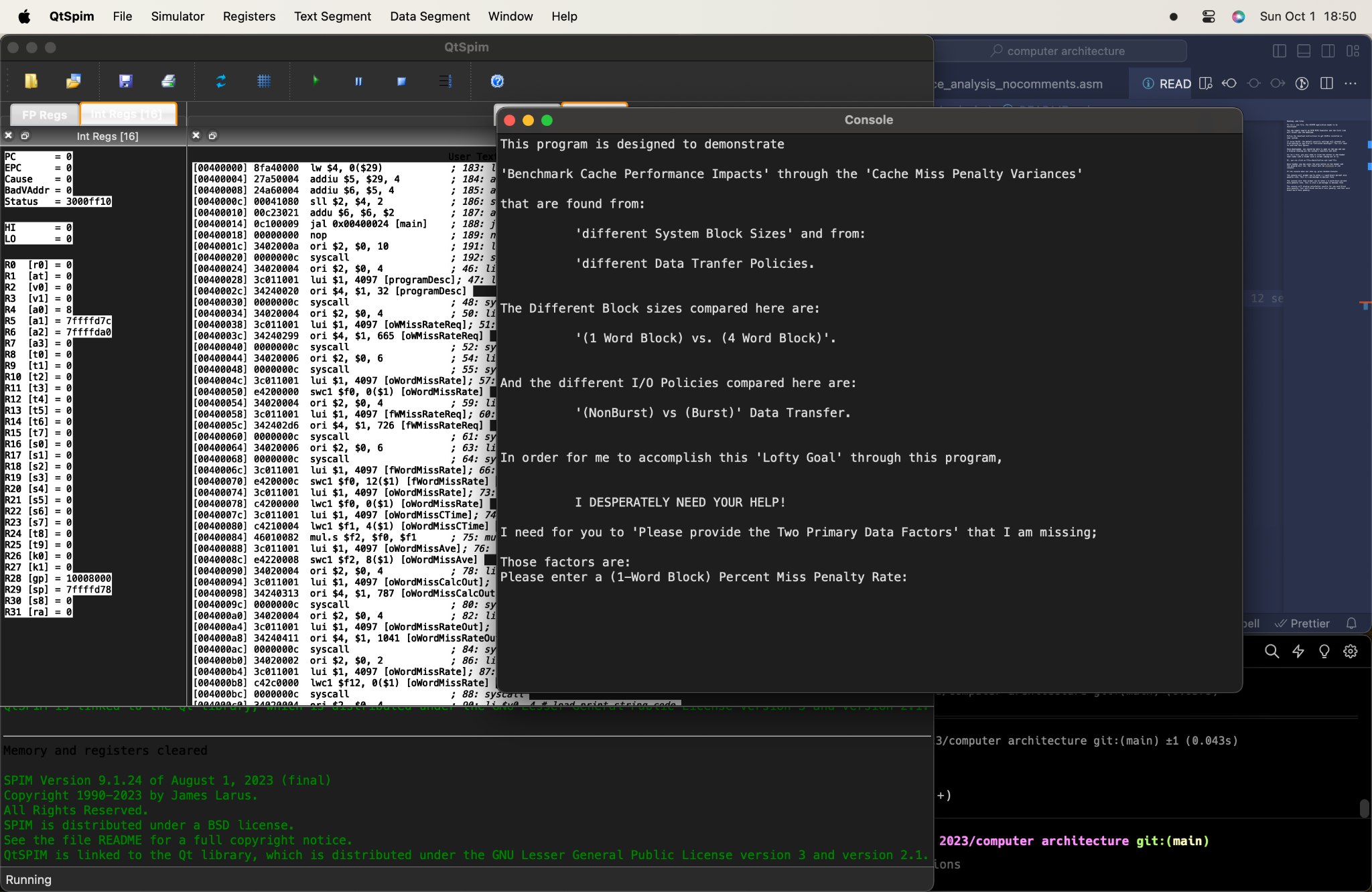
CST-307

Dr. Citro

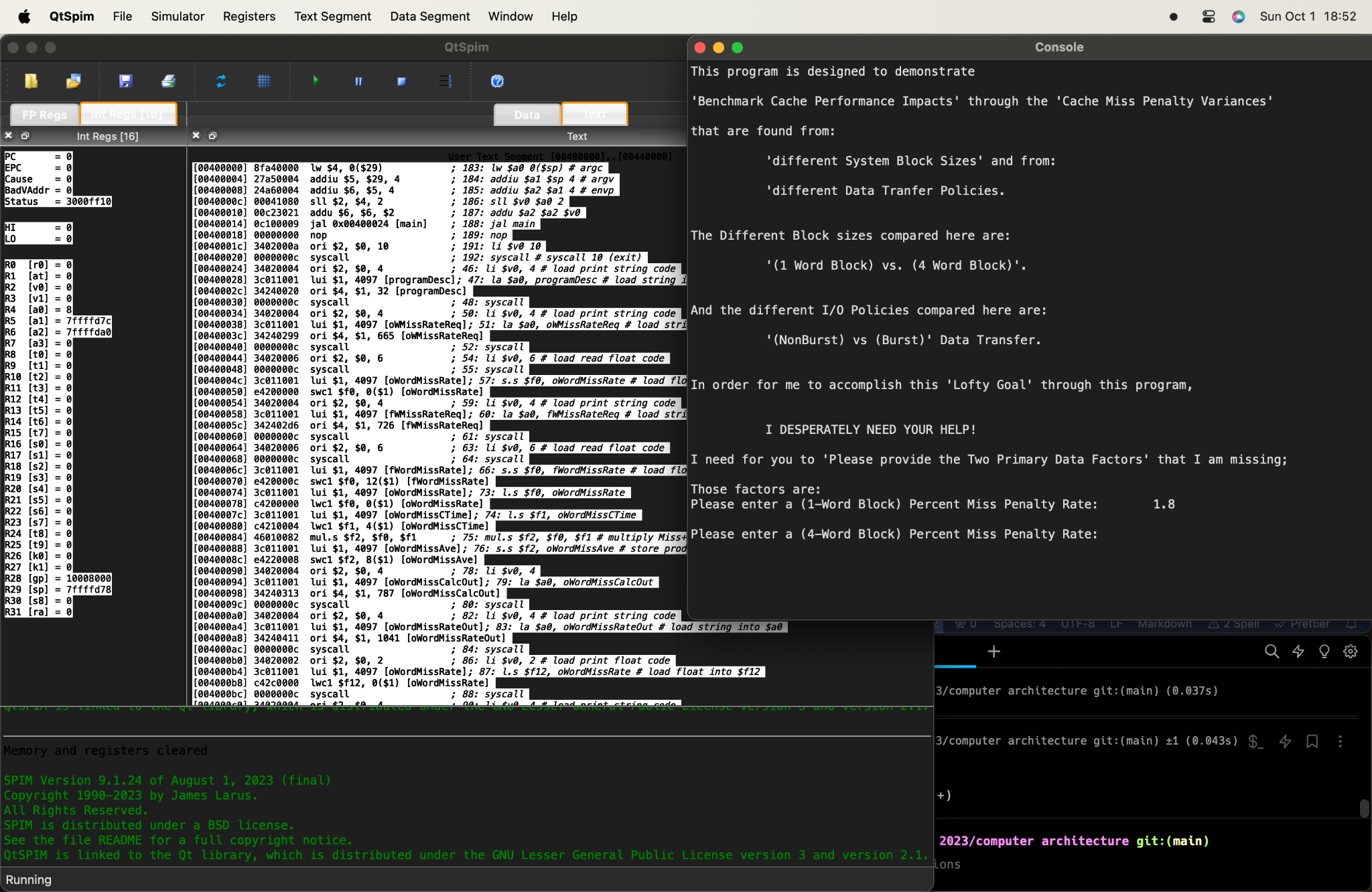
**Benchmark Cache Performance Analysis**

Github CST-307 repository link: <https://github.com/angel-vlzqz/Computer-Architecture>

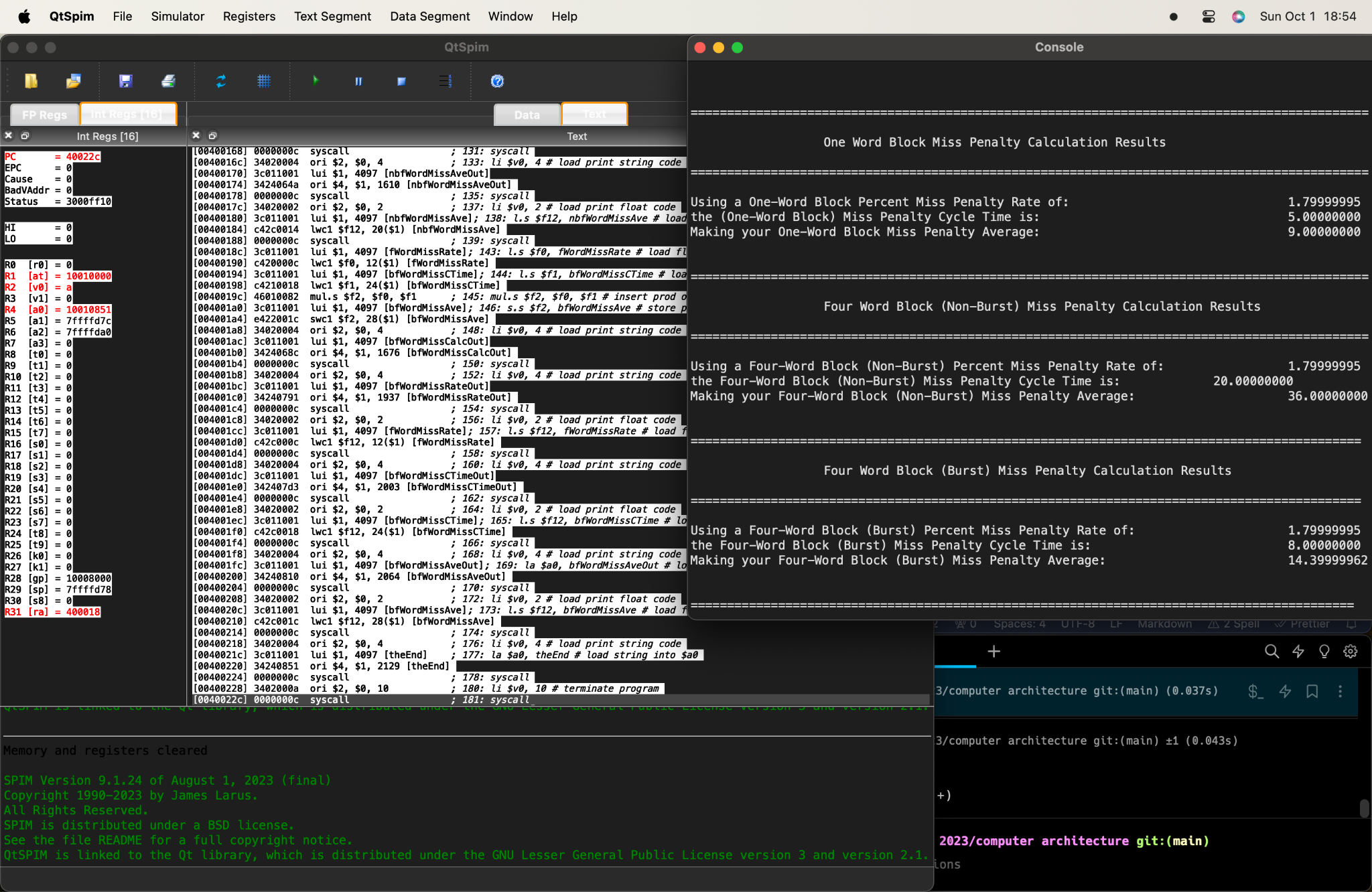
Upon looking at the uncommented code, I will admit that the code looked intimidating. I completed the CLC before starting this assignment to gain experience and knowledge of the register commands. In doing so, I gathered that this program allocates memory to registers and multiplies float values. I find the UI of the program through the console to be efficient and easy to read by the reader.



Upon running the command, the console prompts the user to enter a percentage value in decimal form to compute the 1-word block percent miss penalty.



After entering the first value, the console will prompt the user to enter a second percentage value in decimal form to compute its 4-word block percent miss penalty rates in both burst and non-burst.



After entering a second value, the program will compute its output values in real-time and display the results.

The one-word miss penalty calculations are determined by finding the product of the miss penalty rate provided by the user and the miss penalty cycles. The miss penalty cycle is a constant variable set to 5.

The four-word non-burst miss penalty calculations are determined from the product of the miss penalty rate provided by the user and the miss penalty cycle time set to 20.

The four-word burst miss penalty calculation is determined from the product of the miss penalty rate provided by the user and the miss penalty cycle time set to 8.